Department of Computer Science.
Islamiah College (Autonomous).

Question Bank

Digital Logic Fundamentals

for
I B.Sc.,/B.C.A./ B.Sc., (SW)
First Year – First Semester

(152 Questions)

Unit	No of Questions
I	68
II	17
III	27
IV	20
V	20
Total Questions	**152**

Unit –I: Digital Systems and Binary Numbers – Boolean algebra and Logic Gates.

Number Base Conversions:

1. Convert decimal 153 to octal and binary.
2. Convert decimal 41 to binary, octal and hexadecimal.
3. Convert $(0.6875)_{10}$ to binary.
4. Convert $(4021.2)_5$ to decimal.
5. Convert $(0.513)_{10}$ to octal.
6. Convert $(127.4)_8$, $(B65F)_{16}$, $(110101)_2$ to decimal.
7. Convert the following numbers with the indicated bases to decimal:
   (a) $(4310)_5$ (b) $(198)_{12}$ (c) $(435)_8$ (d) $(345)_6$
8. Convert hexadecimal 2AC5 into decimal, octal and binary.
9. List the octal and hexadecimal numbers from 16 to 32.
10. What is the largest binary number that can be expressed with 16 bits? What are the equivalent decimal and hexadecimal numbers?
11. Convert 64CD to binary and octal.
12. Express the following numbers in decimal:
    $(10110.0101)_2$ (b) $(16.5)_{16}$ (c) $(26.24)_8$ (d) $(DADA.B)_{16}$ (e) $(1010.1101)_2$
13. Convert decimal 27.315 to binary.
14. Convert the binary numbers to hexadecimal and to decimal: (a) $(1.10010)_2$,(b) $(110.010)_2$.
15. Convert C3DF to binary.

Complements of Numbers:

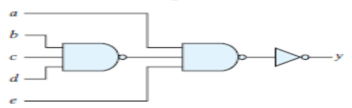
1. Find the 9's and 10's complement of decimal 00000000.
2. Perform +42 - 13 and (-42) + 13 in binary using (i) 1's complement and (ii) 2's complement.
3. Perform 72532 – 3250 using (i) 9’s Complement (ii) 10’s complement.
4. Given the two binary numbers X = 1010100 and Y = 1000011, perform (a) X - Y and (b) Y - X by using 2’s complements, and 1’s complement.
5. Obtain the 1’s and 2’s complements of the following binary numbers:
   (a) 00010000 (b) 00000000 (c) 11011010 (d) 10101010 (e) 10000101 (f) 11111111.
6. Find the 9’s and the 10’s complement of the following decimal numbers:
   (a) (a) 25,478,036 (b) 63, 325, 600 (c) 25,000,000 (d) 00,000,000.
7. Find the 2’s complement and 16’s complement of C3DF.
8. Perform subtraction of the following binary numbers using the 2’s complement
   (a) (a) 10011 - 10010 (b) 100010 – 100110(c) 1001 - 110101 (d) 101000 - 10101
9. Convert decimal +49 and +29 to binary, and using the signed-2’s-complement representation perform
10. (+29) + (-49), (b) (-29) + (+49) and (c) (-29) + (-49).
11. Convert the answers back to decimal andverify that they are correct.
12. What are the three ways to represent –venumbers? Give the range of numbers that could be represented in these methods for four bits.
13. Add and multiply $(110110)_2$ and $(110101)_2$ without converting to decimal.
14. Perform the division in binary: 111011 ÷ 101.
15. Add and multiply the following numbers without converting them to decimal.
    (a) Binary numbers 1011 and 101. (b) Hexadecimal numbers 2E and 34.

Binary Codes:

1. Convert $(185)_{10}$ to BCD and binary.
2. Perform 184 + 576 in BCD.
3. Represent decimal 8620 in (a)BCD (b) excess-3 (c) 2421 code (d) as a binary number.
4. What is the largest binary number that can be obtained with 8-bits? What is its decimal equivalent?
5. What are Weighted, Un-weighted, Self-complementing and Alphanumeric Codes? Give examples.
6. Convert decimal 6,514 to both BCD and ASCII codes. For ASCII, add an even parity bit.
7. Represent decimal numbers 791 and 658 in BCD, and then show the steps necessary to form their sum.
8. Find number of bytes in a system that contains (a) 32K bytes, (b) 64M bytes,(c) 6.4G bytes?
9. How many printing characters are there in ASCII? How many of them are special characters?
10. What bit must be complemented to change an ASCII letter from capital to lowercase andvice versa?
11. The state of a 12-bit register is 100010010111. What is its content if it represents
    (a) BCD (b) excess-3 (c) 8-4-2-1 (d) binary number
12. What is Gray Code? Give its two applications. Write Gray code for decimal 0 to 15.
13. Convert (i) Gray code 101011 into binary (ii) Binary 10111011 into gray code.
14. List the ASCII code for the 10 decimal digits, lower letter alphabets *a* to *z* , Upper case alphabets *A* to *Z*.
15. What is parity bit ? What is MSB and LSB?

Boolean algebra and Logic Gates:

1. Define Boolean algebra with its postulates.
2. State and prove (i) Associative and (ii) Distributive Laws.
3. State and prove De-Morgan's Laws.
4. Define Principle of Duality.
5. What are minterms and maxterms?
6. What are the canonical forms? Give example of its two types.
7. Draw all logic gates with its symbol, algebraic function and truth table.
8. Given two eight-bit strings A = 10110001 and B = 10101100, evaluate the eight-bit result after the following logical operations:(a) AND (b) OR (c) NOT (d) NAND (e) NOR (f) XOR (g) XNOR.
9. Simplify. (i) $xyz + x'y + xyz'$ (ii) $(A + B)'(A' + B')'$ (iii) $(a + b + c)(a'b' + c)$
10. Minimize (i) $(x + y)'(x' + y')$ (ii) $(BC' + A'D)(AB' + CD')$ (iii) $a'bc + abc' + abc + a'bc'$
11. Reduce (i) $A'C' + ABC + AC'$ (ii) $A'B(D' + C'D) + B(A + A'CD)$ (iii) $ABC'D + A'BD + ABCD$
12. Write the Minterms and Maxterms for three binary variables.
13. Find the complement of the functions $F1 = x'yz' + x'y'z$and $F2 = x(y'z' + yz)$
14. Express the Boolean function $F = A + B'C$as a sum of minterms
15. Express the Boolean function $f = xy + x'z$ as a product of maxterms.
16. Find the complement of $F = wx + yz$ then show that $FF' = 0$ and $F + F' = 1$.
17. List the truth table of the function: (a) $F = xy + xy' + y'z$ (b) $F = bc + a'c'$
18. Draw logic diagrams to implement the following Boolean expressions:
    (i) $y = u(x \oplus z) + y'$ (ii) $[(u + x')(y' + z)]$ (iii) $u + x + x'(u + y')$
19. Implement the function $F = xy + x'y' + y'z$ using (i) NAND gates only (ii) NOR gates only.
20. For the function $F = xy'z + x'y'z + w'xy + wx'y + wxy$
    (i) Obtain truth table and logic diagram of F
    (ii) Obtain truth table and logic diagram of simplified expression of F.
21. Convert each of the following to the other canonical form:
    a. F(x, y, z) = ∑ (1, 3, 5) b.F(A, B, C, D) = π (3, 5, 8, 11)
22. Convert the following expressions into sum of products and product of sums:
    (i) $F(A, B, C, D) = B'D + A'D + BD$ (ii) $(u + wx)(x + u'v)$
23. Write Boolean expression and construct the truth table for the circuit



UNIT – II :Gate–Level Minimization.

1. Simplify the Boolean function (i) F (x, y, z) = ∑ (3, 4, 6,7) (ii) F (x, y, z) = ∑ (0, 2, 4, 5, 6)
2. Simplify (i) F(A,B,C,D)=∑(0,2,5,7,8,10,13,15) (ii) F (w, x, y, z) = ∑ (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)
3. Simplify F(A, B, C, D) = (0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15).
4. Minimize (i) F(A,B,C)= π (0,3,6,7) (ii) F(A,B,C,D) = π (3,5,7,8,10,11,12,13)
5. Implement the Boolean function with NAND gates: F (x, y, z) = ∑ (1, 2, 3, 4, 5, 7)
6. Simplify F(w,x,y,z)= ∑ (0,1,2,3,7,8,10) + ∑d(5,6,11,15) and implement using NAND gates only.
7. Simplify the Boolean function (i) $F = A'B'C' + B'CD' + A'BCD' + AB'C'$

   (ii) $x'z + w'xy' + w(x'y + xy')$
8. For the Boolean function= $A'C + A'B + AB'C + BC$. Express this function as (a) sum of minterms.(b) Find the minimal sum-of-products expression.
9. Simplify the Boolean function into (a) sum-of-products form and (b) product-of-sums form

   (i) F (A, B, C, D) = ∑ (0, 1, 2, 5, 8, 9, 10) (ii) $ACD' + C'D + AB' + ABCD$
10. Express $F(x, y, z) = (xy + z)(xz + y)$ into sum of minterms and product of maxterms.
11. Simplify the Boolean function (i) F (w, x, y, z) = ∑ (1, 3, 7, 11, 15) + ∑d(0, 2, 5)

    (ii) F(A,B,C,D) = ∑ (2,4,10,12,14) + ∑d(0,1,5,8)
12. Derive the circuits for a three-bit parity generator and four-bit parity checker using an odd parity bit.
13. Implement the following Boolean expression with exclusive-OR and AND gates:

    $$F = AB'CD' + A'BCD' + AB'C'D + A'BC'D$$
14. Implement the Boolean function F, using (a) NAND gates only (b) NOR gates only.

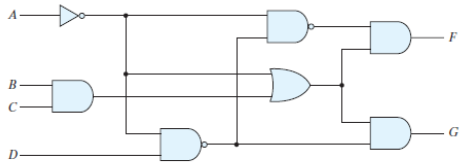
    (i) F(A, B, C, D) = ∑(0, 4, 8, 9, 10, 11, 12, 14). (ii) $f = wx' + y'z' + w'yz'$
15. The truth table of Y in terms of three inputs A,B and C are given. Draw the logic realization of Y using only (i) NAND gates only (ii) NOR gates.

A	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1
Y	1	1	1	0	1	0	0	0

16. Represent all gates using (i) NAND gates only (ii) NOR gates only.
17. Simplify the expression by K-map $AC + B'D + A'CD + ABCD$

UNIT – III : Combinational Logic.

1. Obtain the simplified Boolean expressions for output F and G in terms of the input variables in the circuit



2. Design a combinational circuit with three inputs and one output.
   (a)The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise.
   (b) The output is 1 when the binary value of the inputs is an even number.
3. Design a combinational circuit with three inputs, x ,y and z, and three outputs, A, B and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.
4. A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority circuit by finding the circuit's truth table, Boolean equation, and a logic diagram.
5. Design a combinational circuit that converts a four-bit Gray code to a bit four binary number.
6. Design a code converter that converts a decimal digit from
   a. (a) The 8, 4, –2, –1 code to BCD (b) The 8, 4, –2, –1 code to Gray code.
7. Design a combinational circuit that generates the 9's complement of a BCD digit.
8. Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.
9. Design a combination circuit for BCD to Excess-3 Code.
10. Design a half Adder and a half subtractor with truth table, block diagram and circuit diagram.
11. Implementation of full adder with two half adders and an OR gate.
12. Design a full subtractor with truth table, block diagram and circuit diagram.
13. Design a 4-bit parallel binary adder.
14. Give the difference between a carry and an overflow.
15. Explain the functioning of a BCD adder with block diagram.
16. Design a 4-bit magnitude comparator and explain its working with example.
17. The adder/subtractor circuit has the following values for mode input M and data inputs A and B.

	M	*A*	*B*
(a)	0	0111	0110
(b)	0	1000	1001
(c)	1	1100	1000
(d)	1	0101	1010
(e)	1	0000	0001

   In each case, determine the values of the four SUM outputs, the carry C , and overflow V.
18. With neat diagram and truth table explain encoder and decoder.
19. What is an encoder? Give the truth table of octal to binary encoder.
20. Design a (i) 2 to 4 line decoder (ii) 3 to 8 line decoder.
21. Differentiate between decoder and demultiplexer.
22. Implement a full adder with a decoder.
23. Design an Octal to Binary encoder with truth table.
24. What is a priority encoder? Design a four input priority encoder.
25. Explain Multiplexer. Draw the logic diagram of a four to one line multiplexer.
26. Implement the Boolean function F (A, B, C, D) = $\sum$ (1, 3, 4, 11, 12, 13, 14, 15) using Multiplexer.
27. Construct a 4-to-16-line decoder with five 2-to-4-line decoders

UNIT – IV: Synchronous Sequential Logic.

1. Differentiate between combinational and sequential circuits.
2. Explain S-R latch with logic diagram and truth table.
3. What is a race condition in S-R flip flop?
4. What are synchronous and asynchronous sequential circuits?
5. Draw the logic diagram and truth table of (i) D flip flop (ii) J-K flip flop (iii) T flip-flop.
6. Convert S-R flip-flop to J-K flip-flop. Show the necessary details.
7. How will you convert JK flip-flop into D flip-flop and T flip-flop. Explain applications of D flip-flop and T flip-flop in sequential circuits.
8. Write the characteristic tables and characteristic equations of J-K, D and T-flip flops.
9. Discuss Mealy and Moore state machines.
10. Explain Master-Slave J-K flip flop. What are the advantages of using this over normal flip-flop?
11. Explain the differences among a truth table, a state table, a characteristic table, and an excitation table.
12. Explain the difference among a Boolean equation, a state equation, a characteristic equation, and a flip-flop input equation.
13. What distinguishes a flip-flop from a latch? How do the two circuits differ in function?
14. List two types of edge triggered flip-flops.
15. List one type of asynchronous and three types of synchronous flip-flops.
16. Differentiate D and T Flip Flop.
17. Differentiate level-triggered and edge-triggered flip-flops.
18. Convert the following:(i) S-R to D flipflop (ii) D to S-R flipflop.
19. A sequential circuit has two JK flip-flops A and B and one input *x*. The circuit is described by the following flip-flop input equations:

    $J_A = x$ $K_A = B$

    $J_B = x$ $K_B = A'$

    (a)Derive the state equations A(t+1) and B(t+1) by substituting the input equations for the J and K variables.

    (b) Draw the state diagram of the circuit.
20. A sequential circuit has two JK flip-flops A and B, two inputs *x* and *y*, and one output *z*.

    The flip-flop input equations and circuit output equation are

    $J_A = Bx + B'y'$ $K_A = B'xy'$

    $J_B = A'x$ $K_A = A + xy'$

    $z = Ax'y' + Bx'y'$

    (a) Draw the logic diagram of the circuit.

    (b) Tabulate the state table.

    (c) Derive the state equations for A and B.

UNIT – V: Registers and Counters.

1. Name the four basic types of shift register, and draw a block diagram for each.
2. What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed?
3. The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift?
4. Design a 4-bit Serial adder using shift registers and explain.
5. The 4-bit serial adder uses two four-bit registers. Register A holds the binary number 0101 and register B holds 0111. The carry flip-flop is initially reset to 0. List the binary values in register A and the carry flip-flop after each shift.
6. Design a four-bit shift register with parallel load.
7. Design a four-bit universal shift register and explain its working.
8. Differentiate between asynchronous and synchronous counter.
9. Draw the logic diagram of a four-bit binary ripple countdown counter using flip-flops that trigger (a) on the positive-edge of the clock (b) on the negative-edge of the clock.
10. How many flip-flop will be complemented in a 10-bit binary ripple counter to reach the next count after the following counts? (a) 1001100111 (b) 1111000111
11. Design a four-bit binary synchronous counter with D flip-flops.
12. Design and explain a BCD ripple counter.
13. Design a 4-bit up-down binary counter.
14. Design a four-bit synchronous binary counter.
15. Design a 4-bit binary counter with parallel load and explain.
16. Design a counter with T flip-flops that goes through the binary repeated sequence:0, 1, 3, 7, 6, 4.
17. Using JK flip-flops, design a counter with the repeated binary sequence: 0, 1, 2, 3, 4, 5, 6.
18. Explain (i) Ring Counter (ii) Johnson Counter.
19. Show that a Johnson counter with *n* flip-flops produces a sequence of *2n* states. List the 10 states produced with five flip-flops and the Boolean terms of each of the 10 AND gate outputs.
20. Mention a few applications of (i) Shift Registers (ii) Counters.